DDS-VME Module Configuration Summary

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RF Outputs

RF 1A: Basic frequency curve plus acceleration phase error feedback.

RF 2A: Same as RF 1A but with "A RF" phase control.

RF 3A: Same as RF 1A but with "B RF" phase control.

RF 4A: BPM LO Output (SW6 – Up) / Basic frequency curve (SW6 – DN).

- Phase control includes:
  - Base phase reference adjusted at transition (90deg before transition -90deg after)
  - Paraphase adjustment including
    - Paraphase Curve run at injection.
    - PC1 offset (PC1OFF) that offsets the paraphase curve vertically throughout the entire cycle.
    - PC2 offset (PC2OFF) that offsets the paraphase curve vertically after the designated number of 1 us updates after the initial Booster Cycle Trigger has been reached (PC2CNT). This is typically set just before **transition**.
    - PBR offset (PBROFF) that offsets the paraphase curve vertically after the designated number of 1 us updates after the initial Booster Cycle Trigger has been reached (PBRCNT). This is typically set near the end of the cycle for the purpose of **bunch rotation**.

      * *Paraphase adjustments adjust the A RF and B RF sinewave equal amounts in opposite directions.*

      * *All paraphase functions are disabled if DIP Switch 4 is in the down position.*

  - A RF and B RF phase offset curves. These curves are similar to the frequency curve in that they are defined in ACNET as {time, value} pairs that are interpolated into 1 us updates.
  - RPOS phase shift controlled by an analog phase drive (PSDRV) input. This shifts both the A RF and B RF equal amounts in the same direction.

Digital Inputs, Triggers and Gates

- Trigger Inputs include:
    - Booster Cycle Trigger (DI_1). This triggers the start of the Booster Cycle. This is either a BDOT trigger or a trigger signal with a settable delay from the Booster reset tclk event. Additionally, a Parameter **Curve Delay**, determines how many 20 ns clocks occur between the occurrence of the trigger and the start of the Frequency Curve and Bias Curve playing out.
    - Transition Trigger (DI_2). This trigger signals a paraphase phase shift. A Parameter, X:TRXTIM, determines how long the phase shift takes.
    - Bunch Rotation Enable Gate (DI_3). This gate, in conjunction with the parameter PBRCNT, determines when a paraphase offset is inserted for the sake of bunch rotation near the end of the Booster Cycle. PBRCNT is the number of 1us updates since the start of the paraphase curve that the internal bunch rotation gate goes active. This internal gate AND the Bunch Rotation Enable Gate both have to be active for the bunch rotation offset, PBROFF, to be applied. The Bunch Rotation Enable Gate can be a momentary 1 us pulse since this signal "Sets" an SR flip flop that is reset at the end of the Booster Cycle. With this configuration, the setting of the PBROFF offset is controlled by the particular gate that happens the latest in time.
    - Beam Valid Gate (DI_4). This is equivalent to the current Acceleration Gate signal. This signal is the AND of the Beam Gate which indicates beam in the accelerator and a timed gate signal from ACNET.
    - Bias Gate (DI_1 rear of VME crate). This gates the playing out of the Bias Curve.

Analog Outputs

- Analog Output 1: Scaled representation of the Frequency Curve.
- Analog Output 2: The Bias Curve.
- Analog Output 3: Multiplex Diagnostic Output DAC 3.
- Analog Output 4: Multiplex Diagnostic Output DAC 4.

Analog Inputs

- Analog Input 1: Acceleration phase error feedback.
- Analog Input 2: RPOS Phase Drive feedback.
- Analog Input 3: *reserved*
- Analog Input 4: *reserved*

LED Indicators

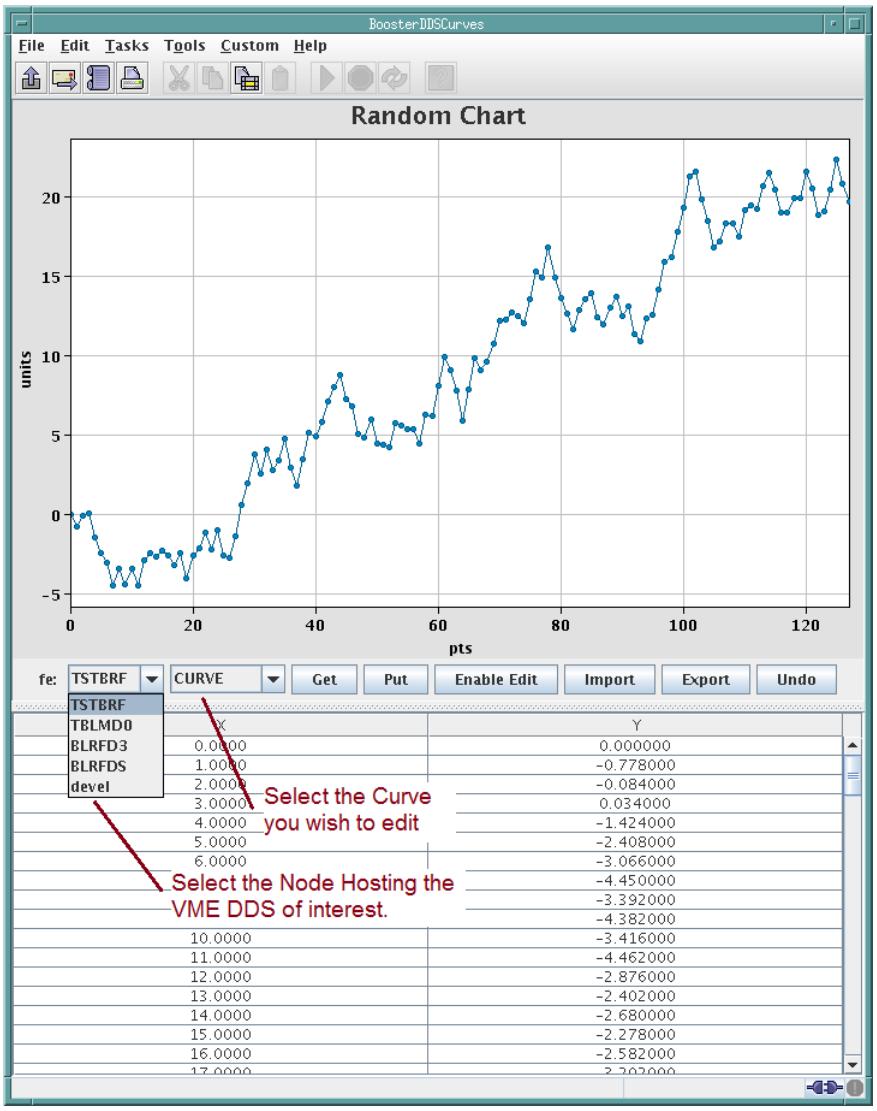
- X LED: VME Bus Activity
- Y LED: Booster Cycle Triggered
- Internal Upper: Acceleration Gate (Beam Gate & ACCEL Gate)
- Internal Lower: *reserved*

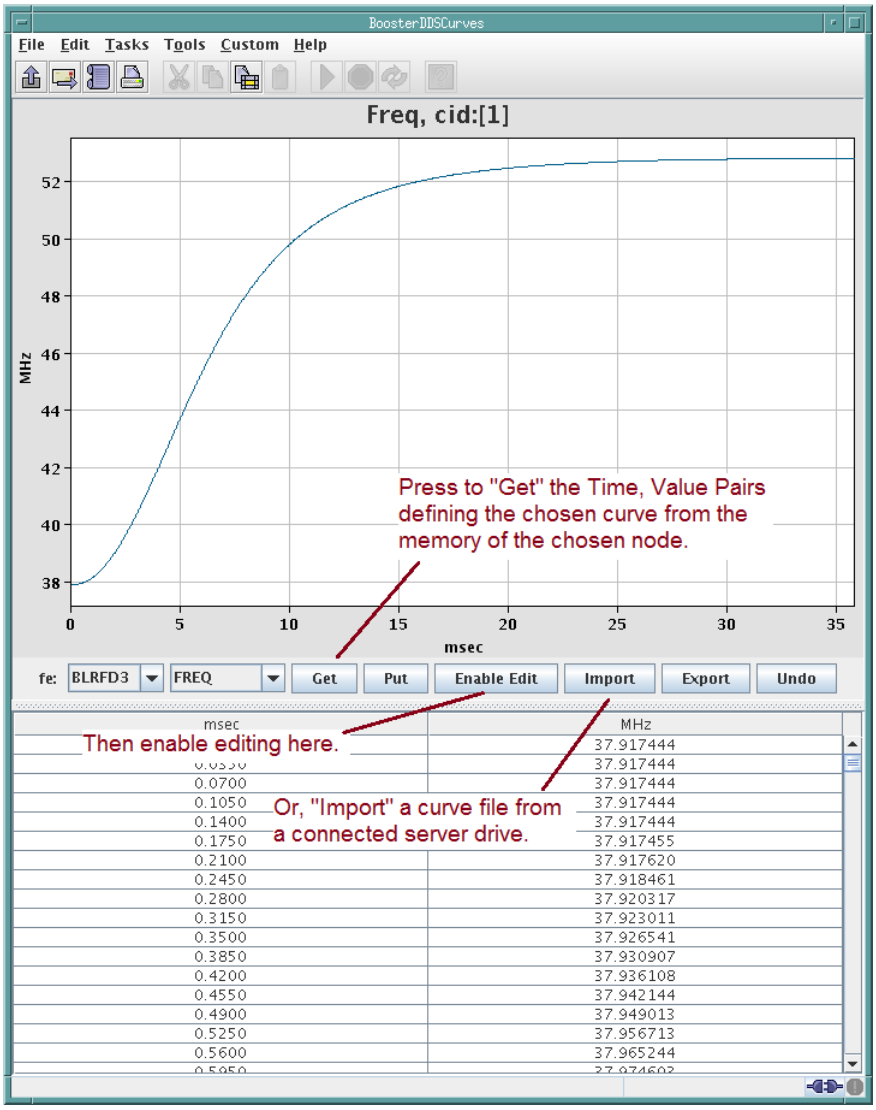
Table 1 ACNET Settable Parameters.

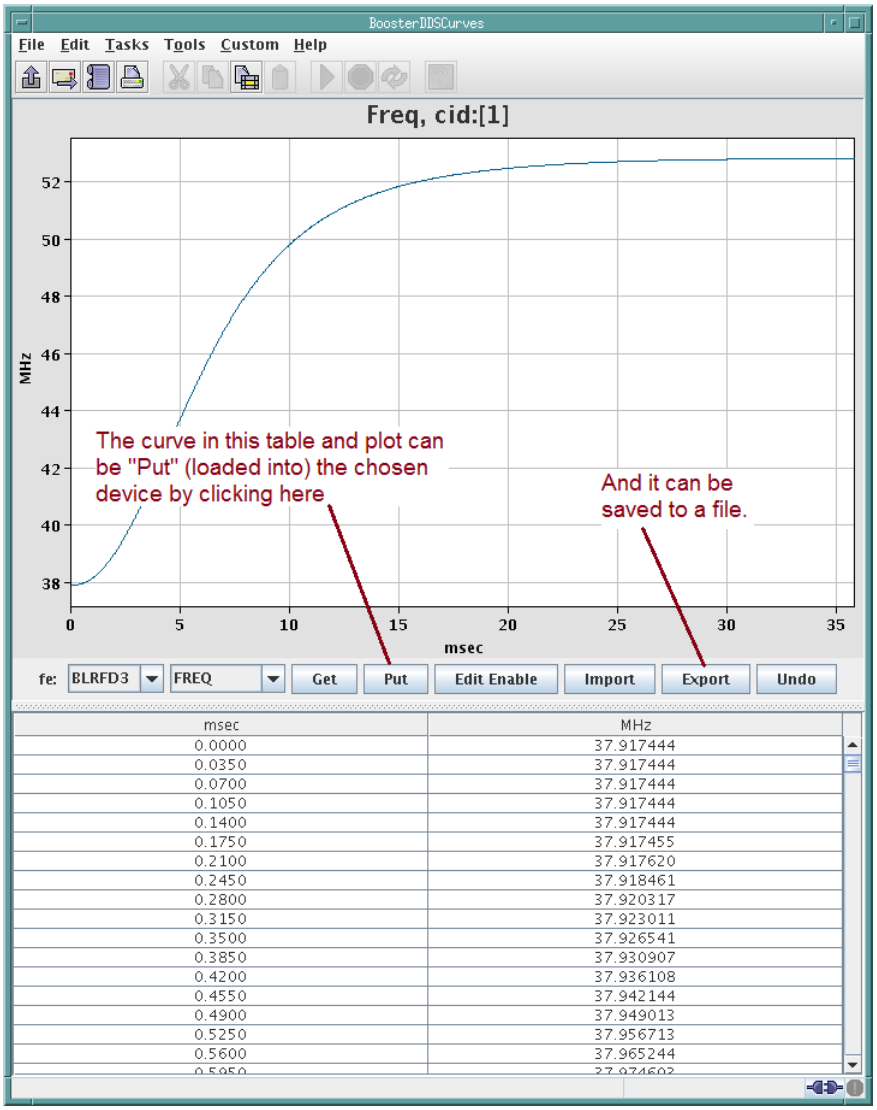
Parameter	ACNET	Scale Factor	Typical Value	Raw Register Value (hex)
0. Injection Frequency	B:INJFRQ	8.94785 Bits/Hz 0.11175869 Hz/Bit	37.933243 MHz	339,420,968 (0x143B2728)
1. No. of Injection Points	B:INJPTS	Number of 4 us points in curve	80 points	80 (0x0050)
2. Curve Run Delay	B:CRVDLY	Micro-Seconds to Number of 20 ns Clocks	100 us	5000 (0x1388)
3. Reverse Steps	B:RVSTPS	Frequency step size for rewinding the Freq. Sweep 8.94785 Bits/Hz	2347 Hz	21,001 (0x5209)
4. Phase Error Gain	B:PHERGN	Scale factor 1	180	180 (0x0B4)
5. Transition Freq. Trigger	B:TTXFRQ	8.94785 Bits/Hz 0.11175869 Hz/Bit	52.800 MHz	472,446,480 (0x1C28F610)
6. RPOS Gain	B:RPOSGN		1	1
7. Phase Error Trim	B:PHETRM	Is summed with the phase error feedback before gain is applied. (32768 = zero, 16 bit offset binary value). Add 32768 to a value of +/- 32767	32784	32784 (0x8010)
8. Transition Interval	B:TRXINT	Number of 1us updates over which transition phase changes occur.	20 us	20 (0x14)
9. Gain Curve Ramp Duration. *(Gain can be ramped from zero to the value "Phase Error Gain" linearly over a specified interval)*	B:GCDUR	Gain curve duration is the interval number times 5.120 us (5.12 = 256 * 0.02)	5.120 us	1
10. Paraphase PC1OFF	B:DC1OFF	Base offset of the entire paraphase curve 182.0444 Bit/Deg 0.005493 Deg/Bit	2.0 Deg	364 (0x16C)
11. Paraphase PC2OFF	B:DC2OFF	Additive offset to the paraphase curve at a given time. 182.0444 Bit/Deg 0.005493 Deg/Bit	2.0 Deg	364 (0x16C)
12. Paraphase PC2 Delay	B:PC2DLY	Number of 1 us updates since the start to when the associated offset is applied.	17 ms	17,000 (0x4268)
13. Paraphase Step Offset Bunch Rotation	B:OFFPBR	Additive offset to the paraphase curve at a given time 182.0444 Bit/Deg 0.005493 Deg/Bit	2.0 Deg	364 (0x16C)
14. Paraphase Step Delay Bunch Rotation	B:PBRDLY	Number of 1 us updates since the start to when the associated offset is applied.	30 ms	30,000 (0x7530)

Curve Development Application

The Frequency, Bias, Paraphase and Phase Offset curve can be created and edited by the following JAVA program. The current “Booster DDS Curves” application is menu item B129.




BoosterDDSCurves
File Edit Tasks Tools Custom Help
Freq, cid:[1]
MHz
msec
Press to "Get" the Time, Value Pairs defining the chosen curve from the memory of the chosen node.
fe: BLRFD3 FREQ Get Put Enable Edit Import Export Undo
Then enable editing here.
Or, "Import" a curve file from a connected server drive.
msec MHz
0.0700 37.917444
0.1050 37.917444
0.1400 37.917444
0.1750 37.917455
0.2100 37.917620
0.2450 37.918461
0.2800 37.920317
0.3150 37.923011
0.3500 37.926541
0.3850 37.930907
0.4200 37.936108
0.4550 37.942144
0.4900 37.949013
0.5250 37.956713
0.5600 37.965244



msec	MHz
0.0000	37.917444
0.0350	37.917444
0.0700	37.917444
0.1050	37.917444
0.1400	37.917444
0.1750	37.917455
0.2100	37.917620
0.2450	37.918461
0.2800	37.920317
0.3150	37.923011
0.3500	37.926541
0.3850	37.930907
0.4200	37.936108
0.4550	37.942144
0.4900	37.949013
0.5250	37.956713
0.5600	37.965244

Sample Curve Files

```
CURVE
Freq
1
1023
8947850.000000
0.000000
0.000000,37.917444
0.035000,37.917444
0.070000,37.917444
0.105000,37.917444
0.140000,37.917444
0.175000,37.917455
0.210000,37.917620
0.245000,37.918461
```

```
CURVE
ParaPhs
7
512
1638.398826
0.000000
0.000000,9.992988
0.001000,9.992988
0.002000,9.992988
0.002000,9.992378
0.004000,9.992378
0.004000,9.992378
0.005000,9.992378
0.007000,9.992378
```

```
CURVE
Bias
2
64
3276.797651
0.000000
0.000000,0.415497
0.008000,0.421906
0.613000,0.438996
0.634000,0.504303
0.685000,0.465546
0.891000,0.476227
0.956000,0.533905
1.018000,0.535126
```

CURVE
Type
Curve Index
No. of Time/Value Pairs
Conversion Multiplier
Conversion Offset
Time/Value Pairs

```
CURVE
Poff1
5
8
1.000000
0.000000
0.000000,-0.500000
5.000000,-0.500000
10.000000,-0.500000
15.000000,-0.500000
20.000000,-0.500000
25.000000,-0.500000
30.000000,-0.500000
35.000000,-0.500000
```

```
CURVE
Poff2
6
8
1.000000
0.000000
0.000000,-0.500000
5.000000,-0.500000
10.000000,-0.500000
15.000000,-0.500000
20.000000,-0.500000
25.000000,-0.500000
30.000000,-0.500000
35.000000,-0.500000
```

SW[7..1] DIP Switch Assignments

SW[3..1] => Module ID used in addressing the module.

SW[4] => Disable paraphase function (when HIGH, down)

SW[5] => Bypass the Bias Gate (force gate on)

SW[6] => Sets RF CH4 from LO to BASE Frq. in UPPER FPGA

SW[7] => Enables the VME control of the processes in the UPPER FPGASW[5] => Bypass Bias Gate

SW[7] AND SW[6] => Enables the Analog IO Control in LOWER FPGA

Control Registers for DDS-VME Evaluation

May 2, 2016

C. Drennan

```
VME_Ctrl_0    : std_logic_vector(23 downto 0) := X"01F100";
```

Requires VME_control_ena (SW7) to be High. SW7 is High in the physical down position.

7	6	5	4	3	2	1	0
Preset Curve Status	Set CTBFREE	Curve Interpolate Trigger	Curve Request Trigger	Backup Trigger	Boot up Trigger	Update Trigger	Verify All

15	14	13	12	11	10	9	8
reserved	reserved	Clear Debug FIFO	Rewind Curves	Update DDS Pulse	Reset Run Curves	Run Curves	reserved

VME_Ctrl_1 : std_logic_vector(23 downto 0) := X"01F104";
(Debug_Select)

31 ... 16	15 ... 8	7 ... 4	3 ... 0
Update Pulse Count to Start Collection	reserved	Debug DAC 3 Data Select	Debug DAC 3 Data Select

VME_Ctrl_1 [3 ... 0]	Signal Name	Description
0000 (0x0)	Paraphase_Sum[15 ... 0]	Paraphase curve plus offsets PC1OFF, PC2OFF, PBROFF.
0001 (0x1)	Paraphase[15 ... 0]	Paraphase curve memory (the base curve).
0010 (0x2)	Phase_Offset_A[15 ... 0]	1 us Interpolated Phase Offset A memory values.
0011 (0x3)	Phase_Offset_B[15 ... 0]	1 us Interpolated Phase Offset B memory values.
0100 (0x4)	DDS_Phase_A[15 ... 0]	Phase Word to A RF DDS, sum of all phase terms
0101 (0x5)	DDS_Phase_B[15 ... 0]	Phase Word to B RF DDS, sum of all phase terms
0110 (0x6)	Reference_Phase[15 ... 0]	Base Phase term that ramps from +90 degrees to -90 degrees at transition.
0111 (0x7)	RPOS_Phase[15 ... 0]	Digitized value of the phase drive feedback.
Others	*reserved*	

VME_Ctrl_1 [7 ... 4]	Signal Name	Description
0000 (0x0)	Pherr_Feedback_OB[15 ... 0]	Acceleration Phase Error Feedback.
0001 (0x1)	Ramped_Pherr_Gain_OB [15 ... 0]	The ramped phase error gain.
0010 (0x2)	Phase_Offset_A[15 ... 0]	1 us Interpolated Phase Offset A memory values.
0011 (0x3)	Phase_Offset_B[15 ... 0]	1 us Interpolated Phase Offset B memory values.
0100 (0x4)	DDS_Phase_A[15 ... 0]	Phase Word to A RF DDS, sum of all phase terms
0101 (0x5)	DDS_Phase_B[15 ... 0]	Phase Word to B RF DDS, sum of all phase terms
0110 (0x6)	Reference_Phase[15 ... 0]	Base Phase term that ramps from +90 degrees to -90 degrees at transition.
0111 (0x7)	RPOS_Phase[15 ... 0]	Digitized value of the phase drive feedback.
Others	*reserved*	

VME_Ctrl_2 : std_logic_vector(23 downto 0) := X"01F108";

31 .. 8	7 ... 4	3 ... 0
reserved	Digital Diag. Mux Select (Level 1)	Digital Diag. Mux Select (Level 2)

See Figure x.x for the output selections.

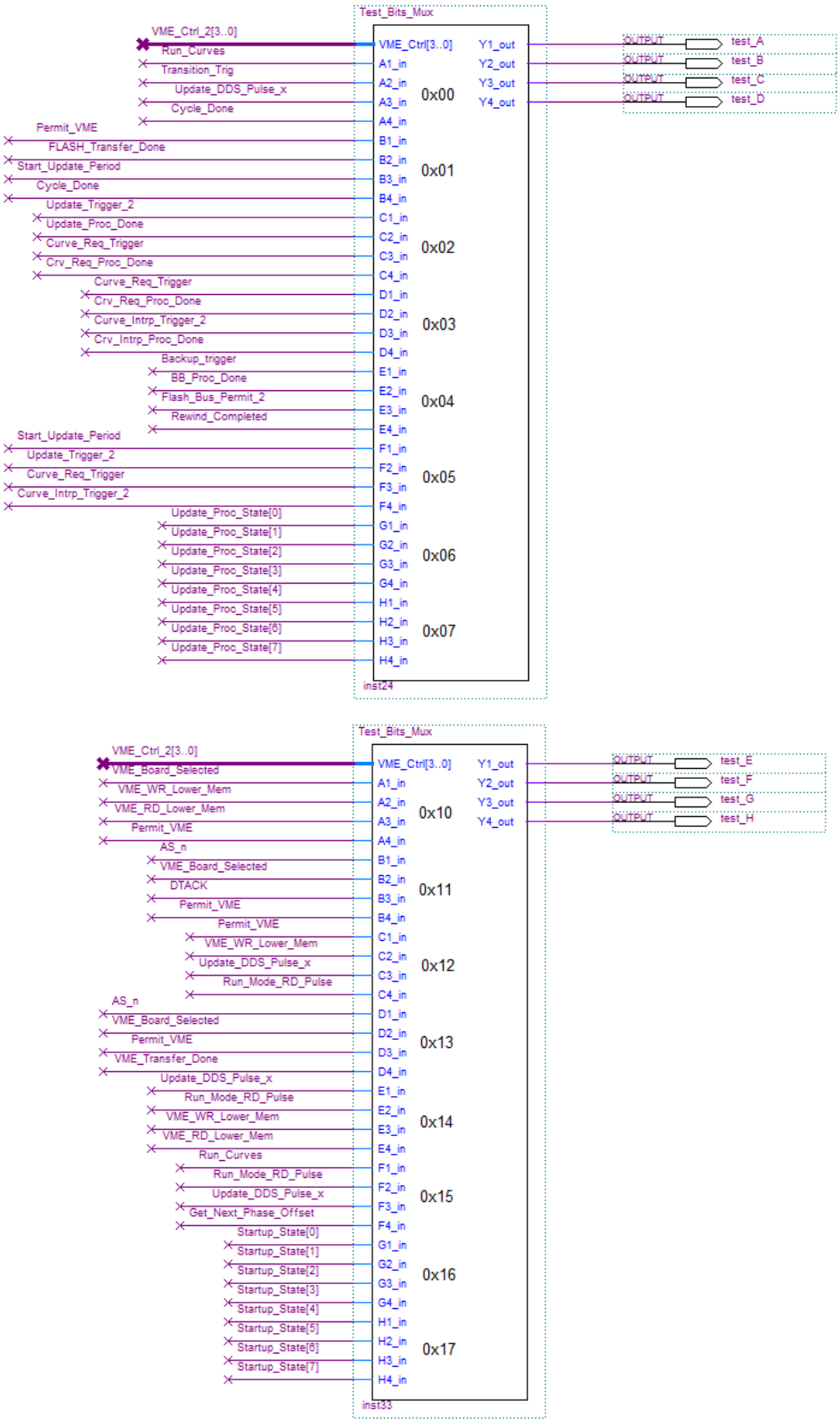


Figure x.x Lower level mux's for diagnostic digital outputs.

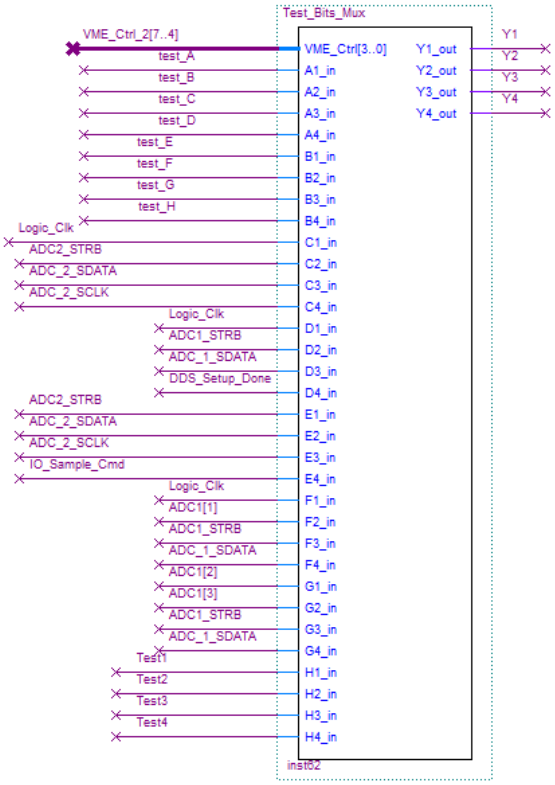


Figure x.x Upper level mux for diagnostic digital outputs.

VME_Ctrl_3 : std_logic_vector(23 downto 0) := X"01F10C";

7	6	5	4	3	2	1	0
					Disable Paraphase	Disable Phase Offset Curves	Disable RPOS Feedback

15	14	13	12	11	10	9	8

Table 1 ACNET Settable Parameters. (Updated 1/13/2017)

Parameter	ACNET	Legacy ACNET Parameter	Old / New Relationship	Scale Factor	Typical Value	Raw Register Value (hex)
0. Injection Frequency	B:INJFRQ (MHz)	B:VFINJ (MHz)	Same units. A small difference in absolute calibration exists. The new system has a better calibration.	8.94785 Bits/Hz 0.11175869 Hz/Bit	37.933243 MHz	339,420,968 (0x143B2728)
1. No. of Injection Points	B:INJPTS (number of 4 uSec steps)	B:VFIDR (uSec)	Multiply INJPTS by 4 uSec to realize the old units.	Number of 4 us points in curve	80 points	80 (0x0050)
2. Curve Run Delay	B:CRVDLY (uSec)	B:VCDLY (clks)	Relationship is mysterious. Tune CRVDLY in steps of 1,2,5 or 10 uSec.	Micro-Seconds to Number of 20 ns Clocks	100 us	5000 (0x1388)
4. Phase Error Gain	B:PHERGN (positive Interger)	Fixed in old system	Values between 100 and 200 have been found reasonable.	Scale factor 1	180	180 (0x0B4)
5. Transition Trigger Frequency.	B:TTXFRQ (MHz)	B:VTRFTG (MHz)	Adjust in the same manner as old system.	8.94785 Bits/Hz 0.11175869 Hz/Bit	52.213 MHz	467,194,092 (0x1BD8D0EC)
7. Phase Error Trim	X:PHETRM (16 bit offset binary number. 32786 = zero)	No equivalent in old system	Do not adjust.	Is summed with the phase error feedback before gain is applied. (32768 = zero, 16 bit offset binary value). Add 32768 to a value of +/- 32767	32784	32784 (0x8010)
9. Gain Curve Ramp Duration. *(Gain can be ramped from zero to the value "Phase Error Gain" linearly over a specified interval)*	X:GCDUR	No equivalent in old system	Do not adjust.	Gain curve duration is the interval number times 5.120 us (5.12 = 256 * 0.02)	5.120 us	1